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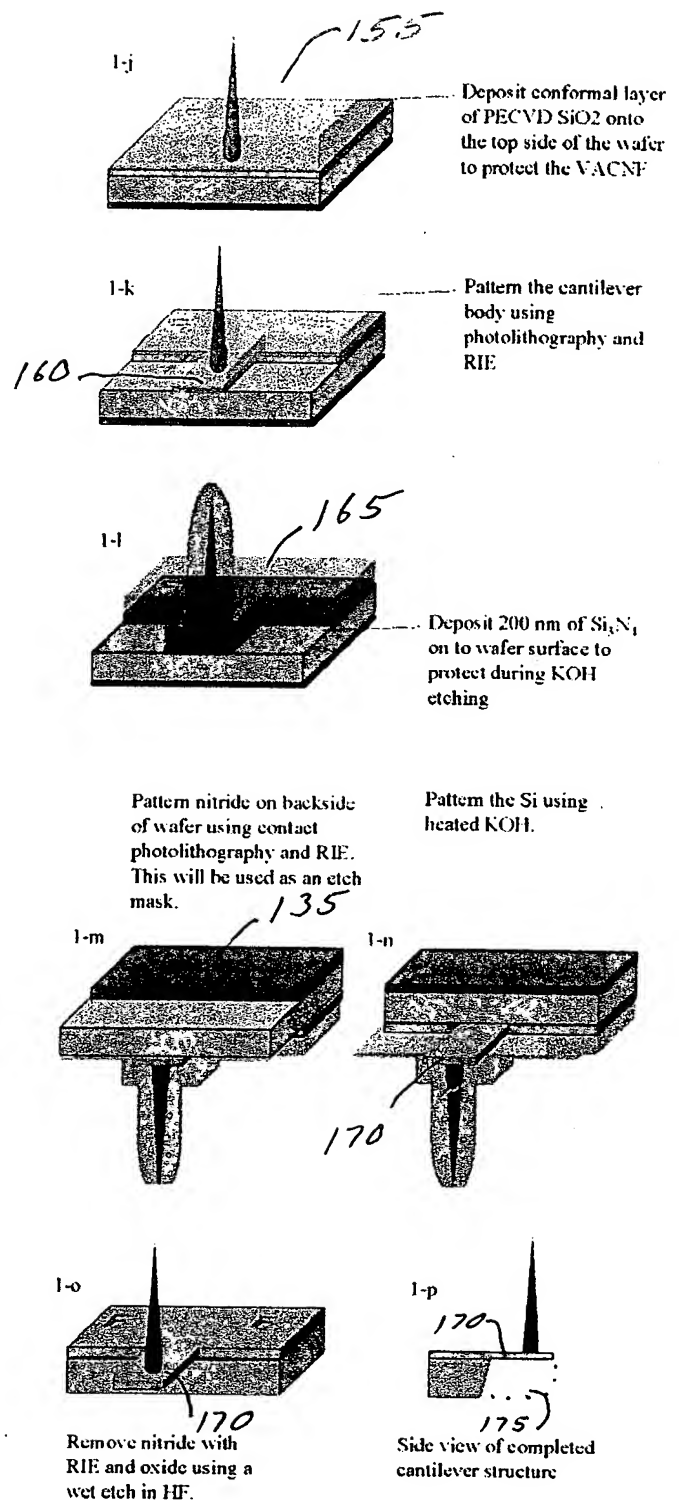
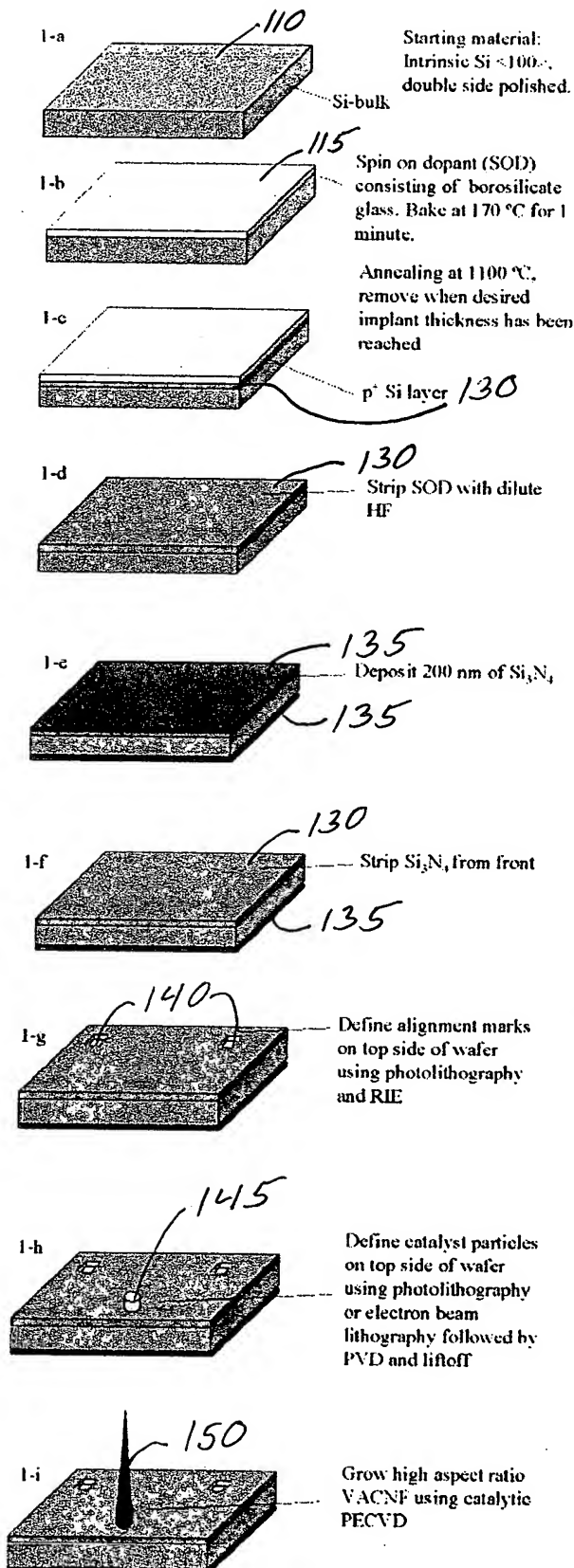
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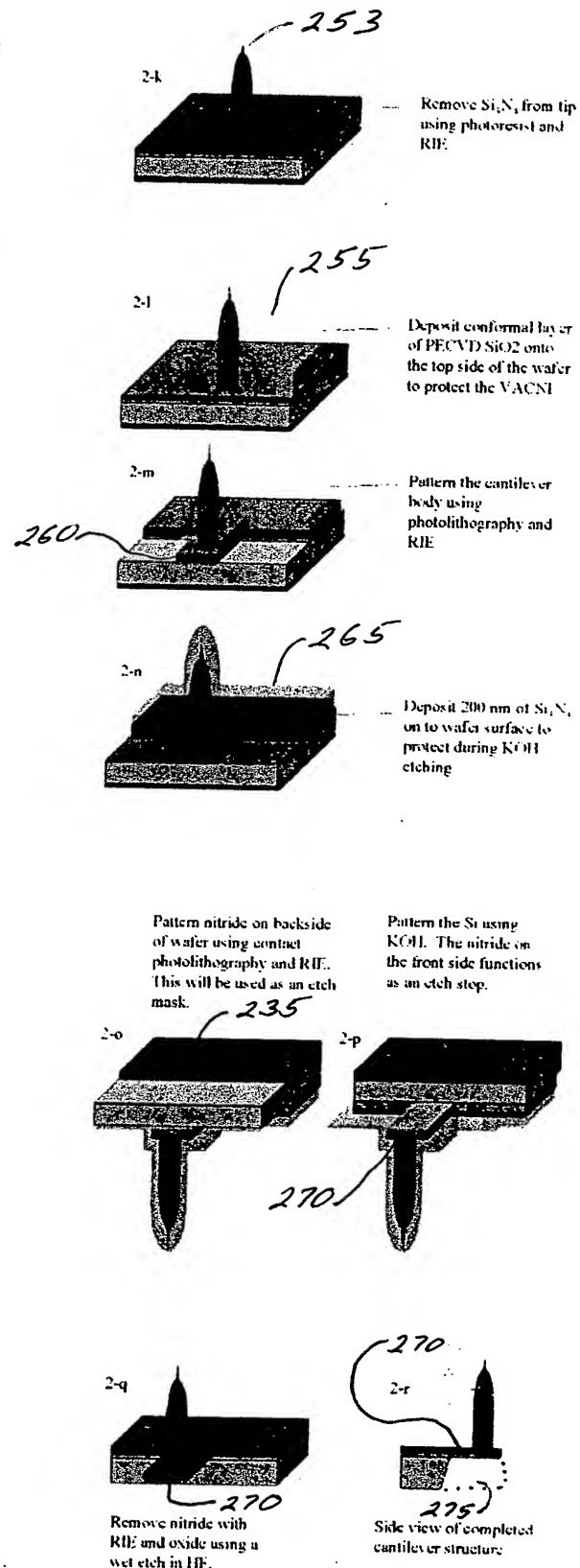
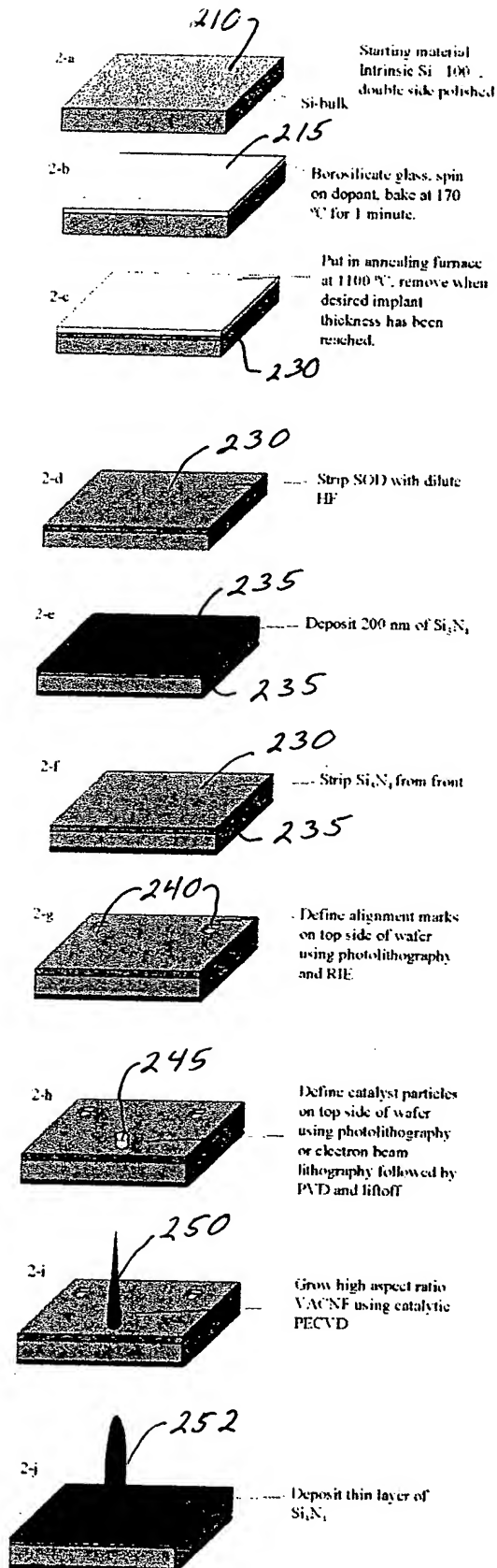
COLORED PHOTOS

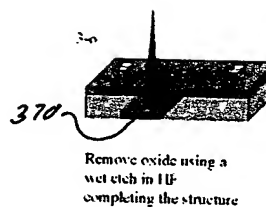
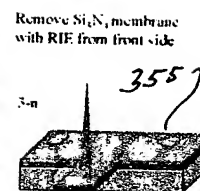
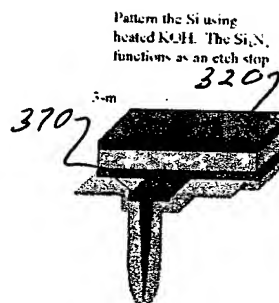
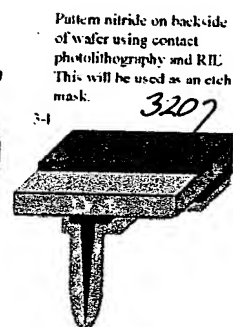
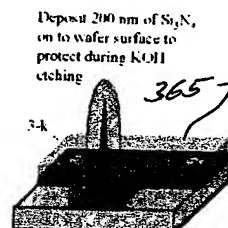
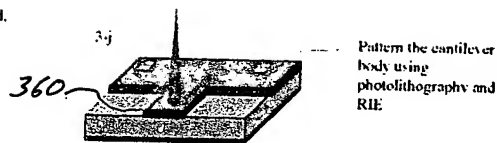
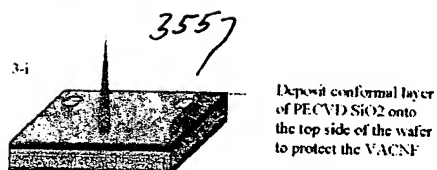
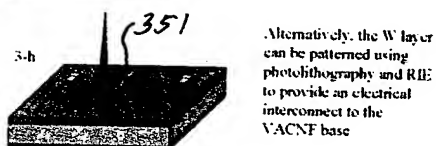
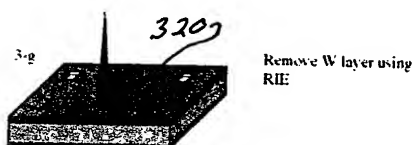
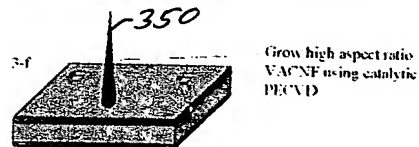
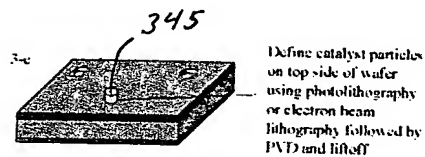
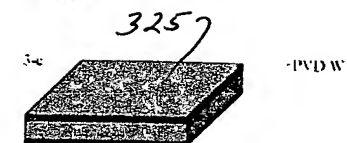
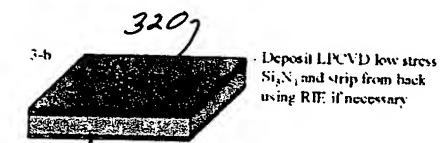
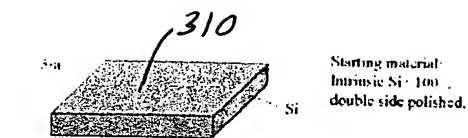
BLACK OR VERY BLACK AND WHITE DARK PHOTOS

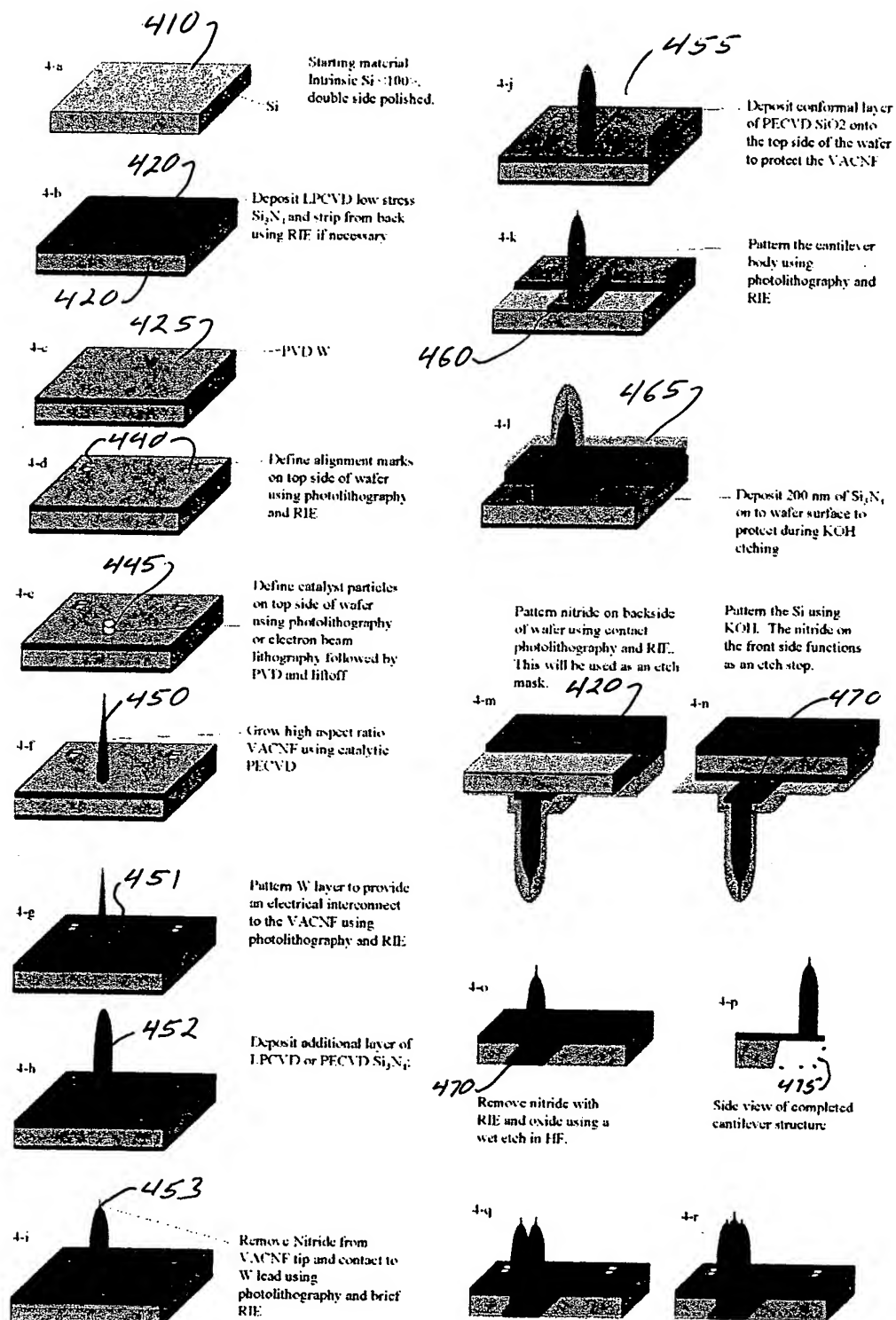
GRAY SCALE DOCUMENTS

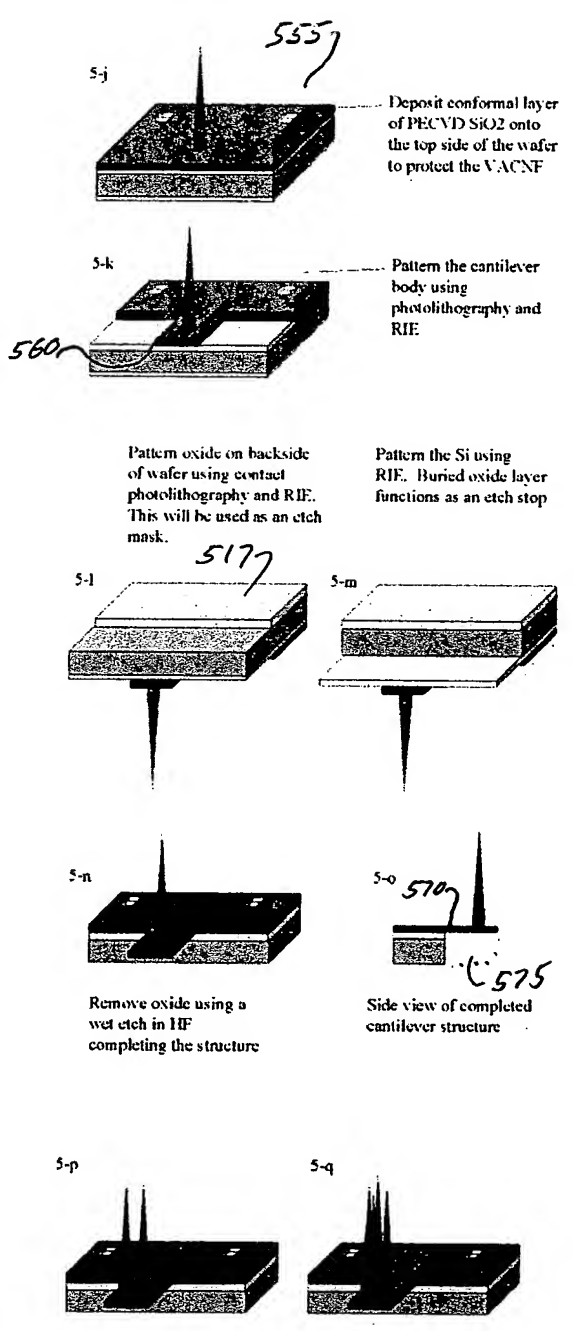
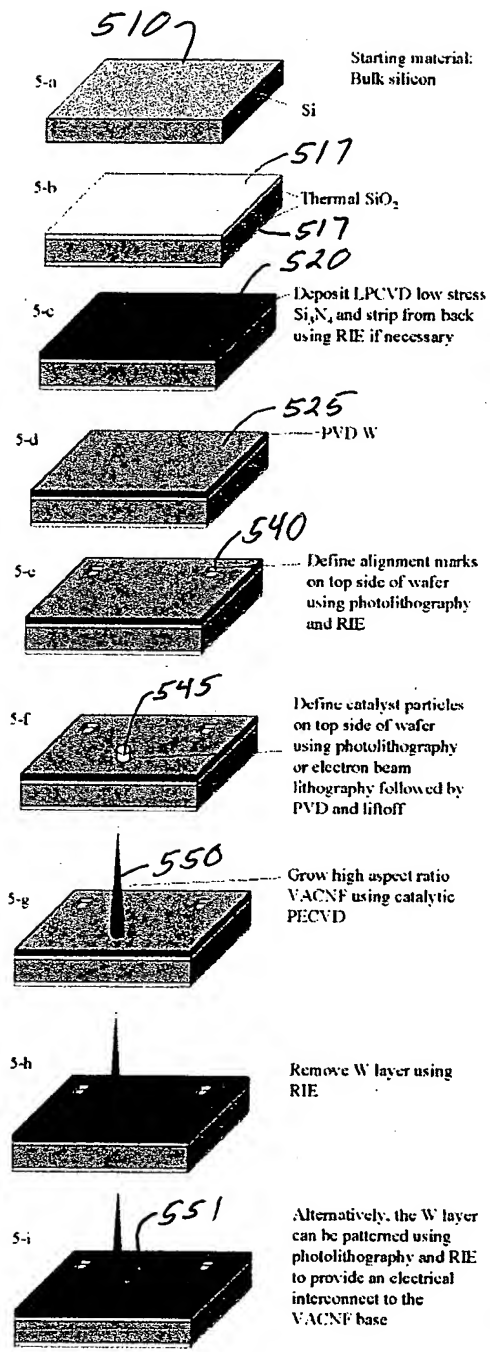
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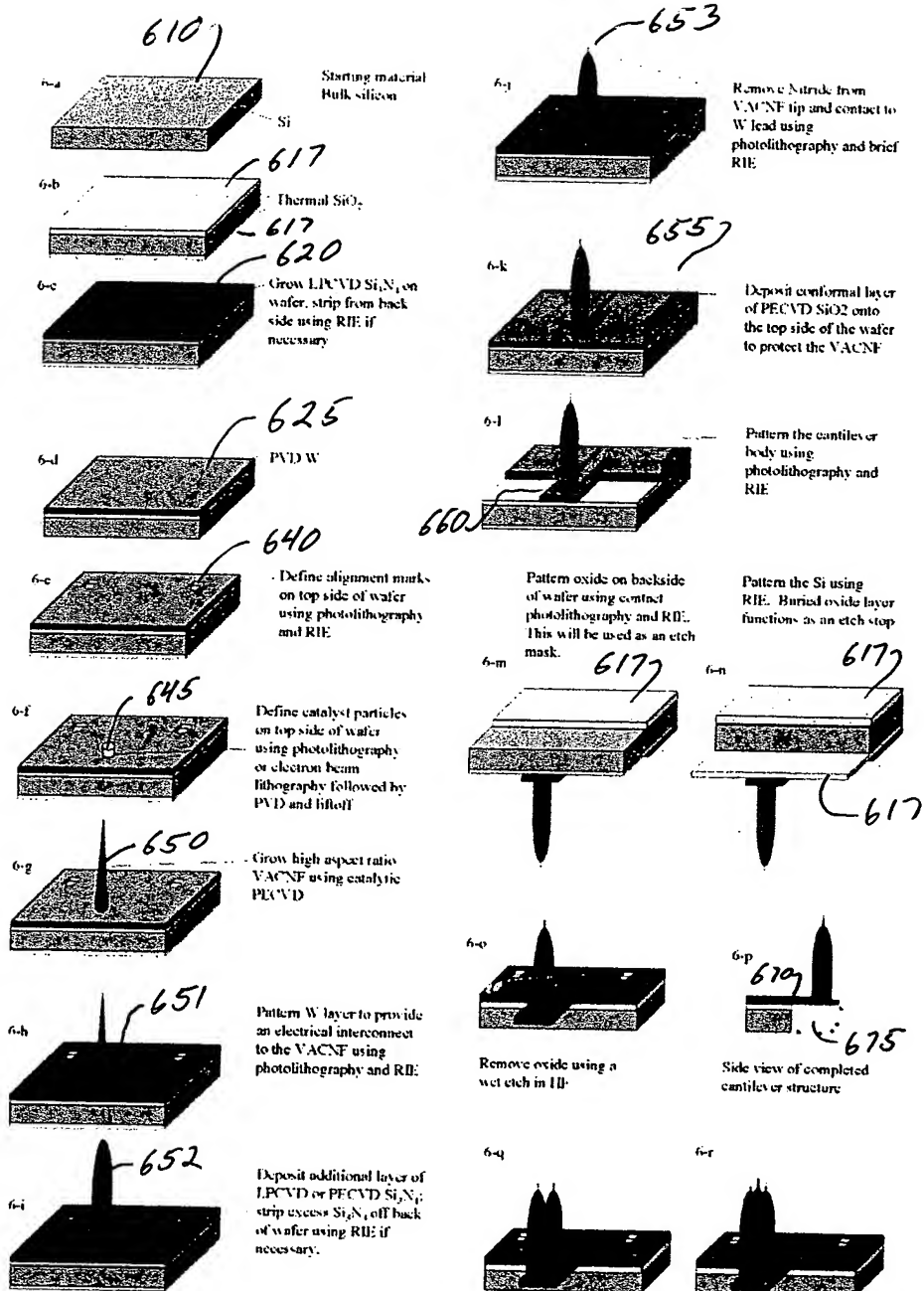












719
717
710

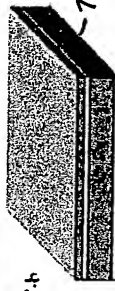
Starting material:
Silicon on insulator
(SOI), double side
polished.

Si
SiO₂
Si-bulk



718

Deposit PECVD SiO₂
masking layer on
back side



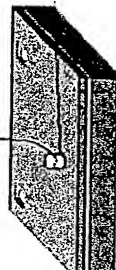
740

Define alignment marks
on top side of wafer
using photolithography
and RIE.



745

Define catalyst particles
on top side of wafer
using photolithography
or electron beam
lithography followed by
PVD and liftoff



750

Grow high aspect ratio
VACNT using catalytic
PECVD



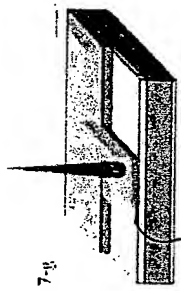
755

Deposit conformal layer
of PECVD SiO₂ onto
the top side of the wafer
to protect the VACNT



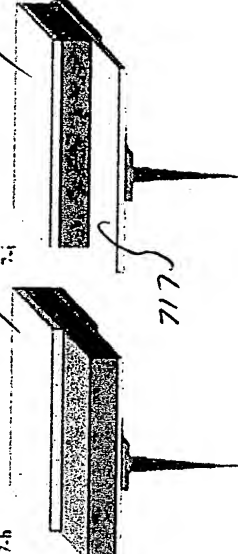
760

Pattern the cantilever
body using
photolithography and
RIE.



787

Pattern the Si using
RIE. The buried oxide
layer functions as an
etch stop.

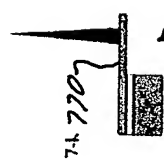
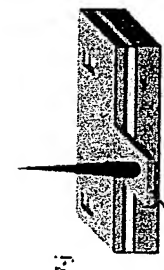


770

Remove oxide using a
wet etch in HCl
completing the structure

775

Side view of completed
cantilever structure



814
811
810

8-a Starting material
Silicon on insulator,
double side polished

8-b Deposit PECVD SiO_2
masking layer on
back side

8-c Define alignment marks
on top side of wafer
using photolithography
and RIE

8-d Define catalyst particles
on top side of wafer
using photolithography
or electron beam
lithography followed by
(PVD) and lift-off

8-e Grow high aspect ratio
VACNF using DC
PECVD

8-f Deposit thin conformal
layer of Si_3N_4

8-g Remove Nitride from
VACNF tip and contact to
W lead using
photolithography and brief
RIE step

855
8-h Deposit conformal layer
of PECVD SiO_2 onto
the top side of the wafer
to protect the VACNF

8-i Pattern the cantilever
body using
photolithography and
RIE

860
8-j Pattern oxide on backside
of wafer using contact
photolithography and RIE.
This will be used as an etch
mask.

8-k Pattern the Si using
RIE. Buried oxide layer
functions as an etch stop

8-l Remove oxide using a
wet etch in III

8-m Side view of completed
cantilever structure

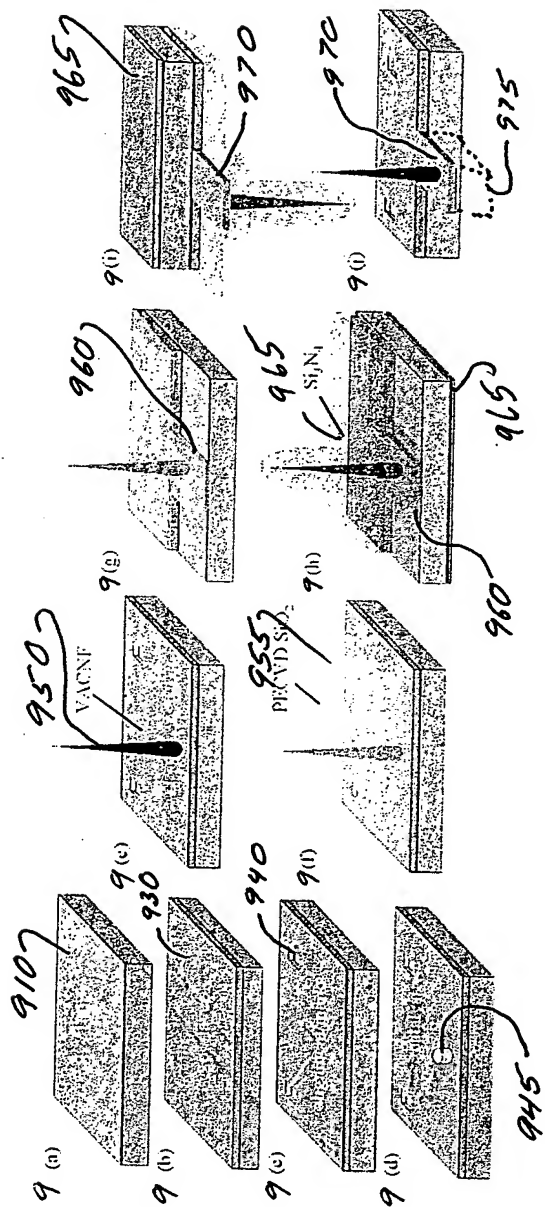


Fig 10A

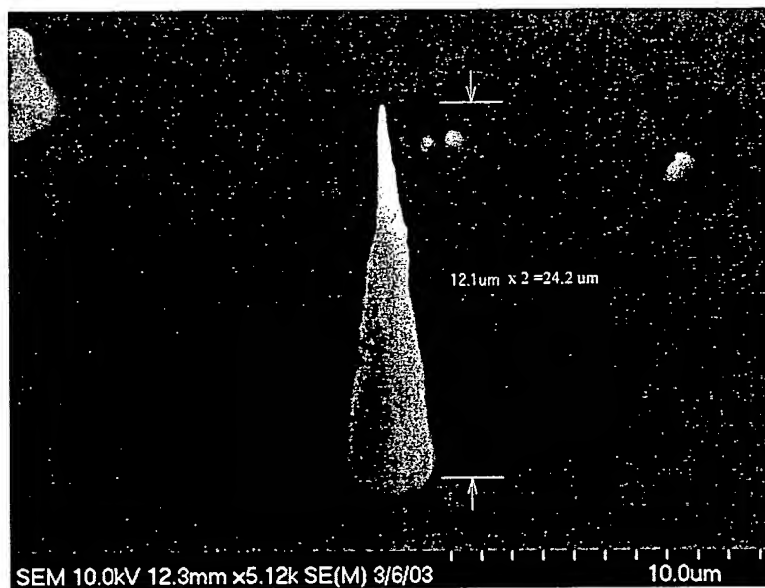


Fig 10B

Fig 11



Fig 12A

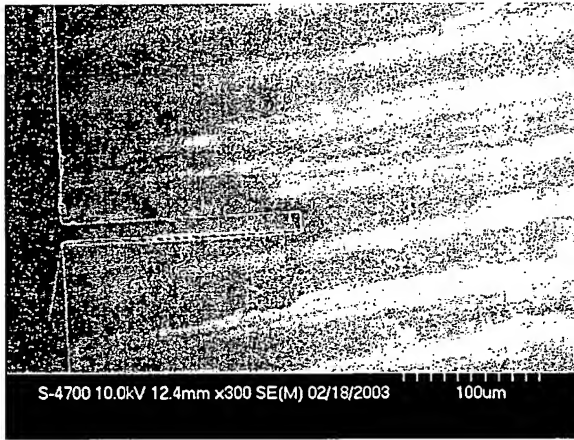


Fig 12B

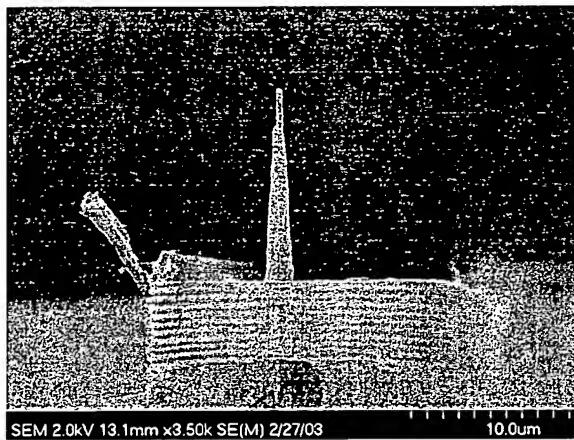
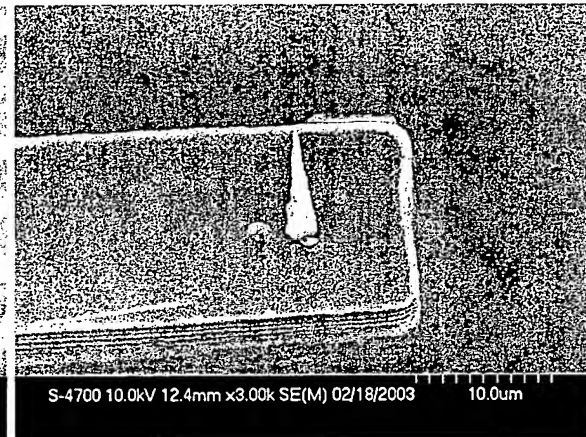


Fig 12C

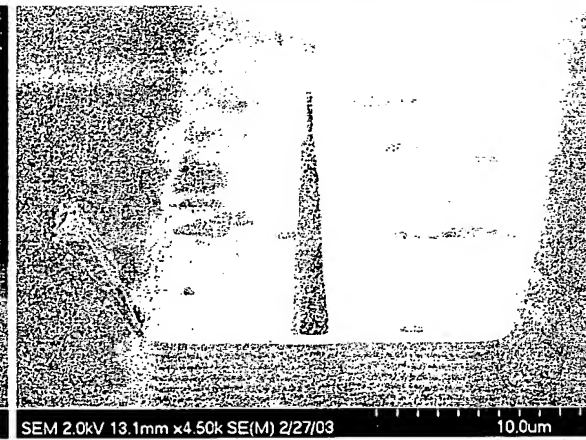


Fig 12D